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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Ajit Dubhashi et al. Date: August 30, 2004

Serial No.: 09/660,813 Group Art Unit: 2829

Filed: September 13, 2000 Examiner: Vinh P. Nguyen

Notice of Allowance Dated: July 30, 2004 Confirmation No. 8167

For POWER SEMICONDUCTOR DEVICE ASSEMBLY WITH INTEGRATED CURRENT SENSING AND CONTROL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attention: Official Draftsperson

SUBMISSION OF FORMAL DRAWINGS

Sir:

Enclosed herewith please find two (2) sheets of replacement drawings containing Figures 1-4 for the above-identified application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, Attn: Official Draftsperson, on August 30, 2004

Samuel H. Weiner
Name of applicant, assignee or Registered Representative

Signature

August 30, 2004

Date of Signature

SHW:fs
Enclosure

Respectfully submitted,

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